## Project Submission Guidelines

The submission should include:

* Cover page including:
  + Subject name & number
  + Project title
  + Lab supervisor’s name
  + Group Member names
* Brief description of your solution to the problem. This would include:
  + **Description** of approach (max 1 page).
  + **Block diagram** of top-level structure.
    - Showing all modules with types and instance names
    - Signal names
    - Port names
  + State transition diagram (STD) or Algorithmic State Machine Diagram (ASMD) for the control block. It is advisable to use the simplified labeling of the STD (if used) to reduce clutter.
  + **A detailed description of all the modules you have designed, highlighting its functionality**.
  + **A detailed description of the testing carried** out (simulation and/or actual hardware)
    - Testbench codes
    - Simulation results
  + **A detailed description on the debugging process**. Bugs you found in your original codes and how you overcome it.
* Listing of VHDL modules.
  + These should be fully commented.
  + These **must** be printed out using a fixed-width font (a print from ISE is suitable).
  + These **must** be properly indented.
  + The use of well-chosen signal, port and module names is expected. The names should reflect the **purpose**  of the signal and **identical** to your group. I would not expect to see **button1** on the state machine module
  + Well-chosen names in general e.g. state names such as **redNS21**, etc rather than **S1**, **S2**.
* Attached the ISE Synthesis report.
* Refer to the project description for guidance on the required operation of the circuit and additional design points to check.
* Pay attention to the guidelines for VHDL and state machines given in lectures. Cryptic code and meaningless comments will LOSE marks.

Only a single submission **per group** is required.